Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1. (currently amended) A method of producing a ~~uniform~~ target wafer thickness profile in a polishing operation, comprising:

(a) providing a model for ~~a~~ wafer polishing that defines a plurality of substantially annular regions on a wafer and identifies a wafer material removal rate in a polishing step for each of the regions; and

(b) polishing a wafer using a polishing recipe that generates a target thickness profile for each region.

Claim 2. (currently amended) A method of controlling surface non-uniformity of a wafer in a polishing operation, comprising:

(a) providing a model for ~~a~~ wafer polishing that defines a plurality of regions on a wafer and a plurality of polishing steps and identifies a wafer material removal rate in a polishing step of a polishing process for each of the regions~~, wherein the polishing process comprises a plurality of polishing~~ steps;

(b) polishing a wafer using a first polishing recipe ~~based upon an incoming wafer thickness profile~~;

(c) determining a wafer thickness profile for the post-polished wafer of step (b); and

(d) calculating an updated polishing ~~recipe~~ model based upon the wafer thickness profile of step (c) and the model of step (a) and updating the first polishing recipe based on the updated model to maintain a target wafer thickness profile.

Claim 3. (currently amended) The method of claim 2, wherein the first polishing recipe is based on the model of step (a) <u>and an initial wafer thickness profile</u><s>to obtain the target wafer thickness profile</s>.

Claim 4. (currently amended) The method of claim 2, wherein the <u>model of step (a) further defines the effect of the tool state on polishing effectiveness</u><s>first polishing recipe is determined emprirically</s>.

Claim 5. (currently amended) The method of claim <s>1 or</s> 2, wherein the plurality of regions in the model of step (a) comprises regions extending radially outward from a center point on the wafer.

Claim 6. (currently amended) The method of claim <u>1 or</u> 5, wherein the model comprises four or more regions.

Claim 7. (currently amended) The method of claim 1 <u>or 2</u>, wherein the polishing of step (b) comprises polishing the wafer at a plurality of polishing stations.

Claim 8. (original) The method of claim 7, wherein the polishing step is carried out at three polishing stations.

Claim 9. (original) The method of claim 7, wherein the polishing recipe at at least two polishing stations is the same.

Claim 10. (original) The method of claim 7, wherein the polishing recipe at at least two polishing stations is different.

Claim 11. (currently amended) The method of claim 7, wherein <s>the</s> calculating the updated polishing <u>model</u> <s>recipe of step (e)</s> comprises calculating updated polishing <s>recipes</s> <u>models</u> for each of the plurality of polishing stations.

Claim 12. (original) The method of claim 11, wherein the updated polishing recipes for each of the plurality of polishing stations accounts for the tool state of the individual polishing stations.

Claim 13. (currently amended) The method of claim 9 or 10, wherein the polishing of step (b) is carried out at a plurality of polishing stations, and wherein ~~the~~ a wafer thickness profile for each of the subsequent polishing stations is determined in step (c) and is used to update the model in step (d)~~provided by the prediction from previous stations~~.

Claim 14. (currently amended) The method of claim 1 or 2, wherein the step of providing a model comprises:

(e) measuring pre-polished wafer thickness in each of a plurality of regions defined on one or more wafers;

(f) polishing the one or more wafers, wherein polishing comprises polishing the one or more wafers in a plurality of polishing steps;

(g) measuring the wafer material removal rate for the one or more wafers at each of the plurality of regions after each of the polishing steps of step (f) ~~(g)~~;

(h) providing a model defining the effect of tool state on polishing effectiveness; and

(i) recording the pre-polished and post-polished wafer thicknesses for each or the regions on a recordable medium.

Claim 15. (original) The method of claim 14, further comprising:

fitting the data to a linear or non-linear curve that establishes a relationship between the material removal rate of a region of the wafer and a polishing parameter of interest.

Claim 16. (currently amended) The method of claim 15 ~~14~~, wherein the polishing parameter comprises polishing time.

Claim 17. (original) The method of claim 16, wherein the polishing parameters further comprise a parameter selected from the group consisting of polishing time, polishing pad down forces and velocity, slurry flow and composition, conditioning time, conditioning disk down forces and velocity, oscillating speeds of both the conditioning disk and the wafer carrier.

Claim 18. (currently amended) The method of claim 1 or 2, wherein the wafer removal for a region j (AR'_j) in the model of step (a) is determined according to the equation:

$$\cancel{AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5;}$$

$$\underline{AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5.}$$

where x_1, x_2, x_3, x_4, and x_5 are the additional parameter values for polishing steps 1, 2, 3, 4, and 5, respectively; t_1, t_2, t_3, t_4, and t_5 are the polishing times for polishing steps 1, 2, 3, 4, and 5, respectively, and c_{a1j} provides the contribution to wafer removal of the variable x in polishing step a in region j; and c_{a2j} provides the contribution to wafer removal of polishing time in polishing step a.

Claim 19. (original) The method of claim 18 wherein the wafer material removal rate profile accounts for tool state by scaling the profile using the scaling factor:

$$\left(1 + k_p \cdot t_p + k_d \cdot t_d + k_{pd} \cdot t_p \cdot t_d\right),$$

where the terms t_p and t_d refer to pad and disk life, respectively, with units of hour; and the terms k_p, k_d and k_{pd} are empirically determined coefficients relating pad and disk life to removal rate.

Claim 20. (currently amended) The method of claim 2, wherein updated polishing model ~~recipe~~ is attained by solving the equation:

$$\min_x f\left(y^{sp}, g(x)\right).$$

where x is a vector of times and other processing parameters corresponding to the

polishing recipe; $g(x)$ is the model for the polishing process, y^{sp} is a vector of the desired average

region wafer thicknesses; and $f(\,y^{sp},\,g(x))$ is a penalty function to penalize the deviation between

the model predictions $g(x)$ and the desired thicknesses y^{sp}.

Claim 21. (original) A method of determining a model for wafer thickness profile,

comprising:

(a) measuring pre-polished wafer thickness in each of a plurality of regions defined on

one or more wafers;

(b) polishing the one or more wafers, wherein polishing comprises polishing the one or

more wafers in a plurality of polishing steps;

(c) measuring the wafer material removal rate for the one or more wafers at each of the

plurality of regions after each of the polishing steps of step (b);

(d) providing a model defining the effect of tool state on polishing effectiveness; and

(e) recording the pre-polished and post-polished wafer thicknesses for each or the

regions on a recordable medium.

Claim 22. (original) The method of claim 21, further comprising:

fitting the data to a linear or non-linear curve that establishes a relationship between the

material removal rate of a region of the wafer and a polishing parameter of interest.

Claim 23. (original) The method of claim 22, wherein the polishing parameter

comprises polishing time.

Claim 24. (original) The method of claim 23, wherein the polishing parameters further

comprise a parameter selected from the group consisting of polishing time, polishing pad down

forces and velocity, slurry flow and composition, conditioning time, conditioning disk down

forces and velocity, oscillating speeds of both the conditioning disk and the wafer carrier.

Claim 25. (currently amended) The method of claim 21 wherein the wafer material

removal for a region j (AR'_j) in the model of step (a) is determined according to the equation:

$$\cancel{AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5,}$$

$$\underline{AR'_j = (c_{11j} \cdot x_1 + c_{12j}) \cdot t_1 + (c_{21j} \cdot x_2 + c_{22j}) \cdot t_2 + (c_{31j} \cdot x_3 + c_{32j}) \cdot t_3 + (c_{41j} \cdot x_1 + c_{42j}) \cdot t_4 + (c_{51j} \cdot x_5 + c_{52j}) \cdot t_5,}$$

where x_1, x_2, x_3, x_4, and x_5 are the additional parameter values for polishing steps 1, 2, 3,

4, and 5, respectively; t_1, t_2, t_3, t_4, and t_5 are the polishing times for polishing steps 1, 2, 3, 4, and

5, respectively, and c_{a1j} provides the contribution to wafer removal of the variable x in polishing

step a in region j; and c_{a2j} provides the contribution to wafer removal of polishing time in

polishing step a.

Claim 26. (original) The method of claim 21 wherein the wafer material removal rate

profile accounts for tool state by scaling the profile using the scaling factor:

$$\left(1 + k_p \cdot t_p + k_d \cdot t_d + k_{pd} \cdot t_p \cdot t_d\right),$$

where the terms t_p and t_d refer to pad and disk life, respectively, with units of hour; and

the terms k_p, k_d and k_{pd} are empirically determined coefficients relating pad and disk life to

removal rate.

Claim 27. (currently amended) The method of claim 22, wherein ~~a~~ the model is

determined using less than 10 wafers.

Claims 28. (withdrawn) An apparatus for polishing substrates, comprising:

a carrier assembly having a plurality of arms for holding a wafer positionable over a

plurality of planarizing surfaces of a plurality of polishing pads;

controlling means capable of controlling an operating parameter of the polishing process;

and

a controller operatively coupled to the controlling means, the controller operating the

controlling means to adjust the operating parameter of the polishing process as a function of a

model for a wafer thickness profile, the model comprising:

defining a polishing model that defines a plurality of regions on a wafer and identifies a

wafer material removal rate in a polishing step of a polishing process for each of the regions,

wherein the polishing process comprises a plurality of polishing steps.

29.   (withdrawn) The apparatus of claim 28, wherein the model defines wafer

removal for a region j (AR'_j) in the wafer material removal rate model is determined according to

the equation:

$$AR'_j = (c_{11j} \cong x_1 + c_{12j}) \cong t_1 + (c_{21j} \cong x_2 + c_{22j}) \cong t_2 + (c_{31j} \cong x_3 + c_{32j}) \cong t_3 + (c_{41j} \cong x_1 + c_{42j}) \cong t_4 + (c_{51j} \cong x_5 + c_{52j}) \cong t_5,$$

where x_1, x_2, x_3, x_4, and x_5 are the additional parameter values for polishing steps 1, 2, 3,

4, and 5, respectively; t_1, t_2, t_3, t_4, and t_5 are the polishing times for polishing steps 1, 2, 3, 4, and

5, respectively, and c_{a1j} provides the contribution to wafer removal of the variable x in polishing

step a in region j; and c_{a2j} provides the contribution to wafer removal of polishing time in

polishing step a.

30.   (withdrawn) A computer readable medium comprising instructions being

executed by a computer, the instructions including a computer-implemented software application

for a chemical mechanical polishing process, the instructions for implementing the process

comprising:

(a) receiving data from a chemical mechanical polishing tool relating to the wafer

removal rate of at least one wafer processed in the chemical mechanical polishing process; and

(b) calculating, from the data of step (a), updated polishing recipe, wherein the updated

polishing recipe is calculated by determining the difference between an output of a wafer

material removal rate model and the data of step (a).

31.   (withdrawn) The medium of claim 28, wherein the model for a wafer material

removal rate defines a plurality of regions on a wafer and identifies a wafer material removal rate

in a polishing step of a polishing process for each of the regions, wherein the polishing process

comprises a plurality of polishing steps.

32.   (withdrawn) The medium of claim 30, wherein the wafer removal for a region j

(AR'_j) in the wafer material removal rate model is determined according to the equation:

$$AR'_j = (c_{11j} \cong x_1 + c_{12j}) \cong t_1 + (c_{21j} \cong x_2 + c_{22j}) \cong t_2 + (c_{31j} \cong x_3 + c_{32j}) \cong t_3 + (c_{41j} \cong x_1 + c_{42j}) \cong t_4 + (c_{51j} \cong x_5 + c_{52j}) \cong t_5,$$

where x_1, x_2, x_3, x_4, and x_5 are the additional parameter values for polishing steps 1, 2, 3,

4, and 5, respectively; t_1, t_2, t_3, t_4, and t_5 are the polishing times for polishing steps 1, 2, 3, 4, and

5, respectively, and c_{a1j} provides the contribution to wafer removal of the variable x in polishing

step a in region j; and c_{a2j} provides the contribution to wafer removal of polishing time in

polishing step a.

33.   (withdrawn) A system for producing a uniform wafer thickness profile in a

polishing operation, comprising:

(a) means for modeling wafer polishing that defines a plurality of regions on a wafer and identifies a wafer material removal rate in a polishing step of a polishing process for each of the regions, wherein the polishing process comprises a plurality of polishing steps;

(b) polishing means for polishing a wafer using a first polishing recipe based upon an incoming wafer thickness profile;

(c) measuring means for determining a wafer thickness profile for the post-polished wafer of step (b); and

(d) calculating means for calculating an updated polishing recipe based upon the wafer thickness profile of step (c) and the model of step (a) to maintain a target wafer thickness profile.